PAT-NO: JP02002251301A
DOCUMENT-IDENTIFIER: JP 2002251301 A
TITLE: CPU MONITORING CIRCUIT

PUBN-DATE: September 6, 2002

INVENTOR-INFORMATION:

NAME	COUNTRY
HOSHIKAWA, CHIKASHIGE	N/A

ASSIGNEE-INFORMATION:

NAME	COUNTRY
TOYOTA MOTOR CORP	N/A

APPL-NO: JP2001047361
APPL-DATE: February 22, 2001

INT-CL (IPC): G06F011/30 , G06F001/28 , G06F001/24 , G05F001/10 , G05F003/30

ABSTRACT:

PROBLEM TO BE SOLVED: To prevent monitoring time for detecting a CPU clock signal from fluctuating even though battery voltage fluctuates with respect to a CPU monitoring circuit.

SOLUTION: A WD monitoring circuit 12 is provided with a capacitor 26 that is discharged in a normal state and charged when a WD signal issued by a CPU 10 in a prescribed cycle is supplied, and a comparator with hysteresis 24 for comparing the voltage of the capacitor 26 with a reference voltage and requesting the CPU 10 to perform reset start when the voltage of the capacitor 26 falls down to the reference voltage. The reference voltage is made to be the voltage based on bandgap voltage VOUT.